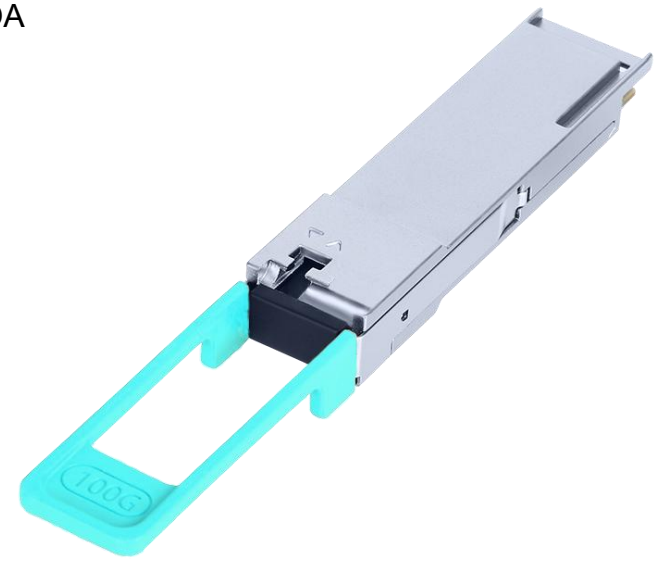
QFP-BLxxHG-80DC

100Gb/s BIDI QSFP28 ZR4 Transceiver

FEATURES

- Supports 103.125Gb/s aggregate bit rate
- Built-in 4-channel Clock and Data Recovery (CDR) in TX and RX
- LAN WDM EML laser and PIN receiver with SOA
- Up to 80km reach for G.652 SMF
- Hot pluggable 38 pin electrical interface
- QSFP28 MSA compliant
- BIDI LC optical receptacle
- RoHS-10 compliant and lead-free
- Excellent EMI performance
- Single +3.3V power supply
- Maximum power consumption 5.5W
- Case operating temperature 0 ~ 70℃



APPLICATIONS

- 100GBASE-ZR4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Telecom networking

DESCRIPTIONS

QFP-BLxxHG-80DC is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial inter-face. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	V_{CC}	-0.3	4.0	V	
Relative Humidity (non-condensation)	RH	15	85	%	
Damage Threshold	TH_d	6.5		dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TOP	0		70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			25.78125		Gb/s	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance (SMF)	D			80	km	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Power Consumption	p			5.5	W	
Supply Current	Icc			1585	mA	
Transmitter (each Lane)						
Input differential impedance	Rin		100		Ω	
Differential Termination Mismatch				10	%	
Differential Data Input Amplitude	Vin, PP	180		1000	mV	
LPMode, Reset and ModSelL	V_{IL}	-0.3		0.8	V	
	V_{IH}	2		Vcc+0.3	V	

Receiver						
Differential Data Output Amplitude	Vout, PP	350		900	mV	
Differential Termination Mismatch				10	%	
Transition Time, 20 to 80%		9.5			ps	
ModPrsL and IntL	VOL	0		0.4	V	
	VOH	Vcc-0.5		Vcc+0.3	V	

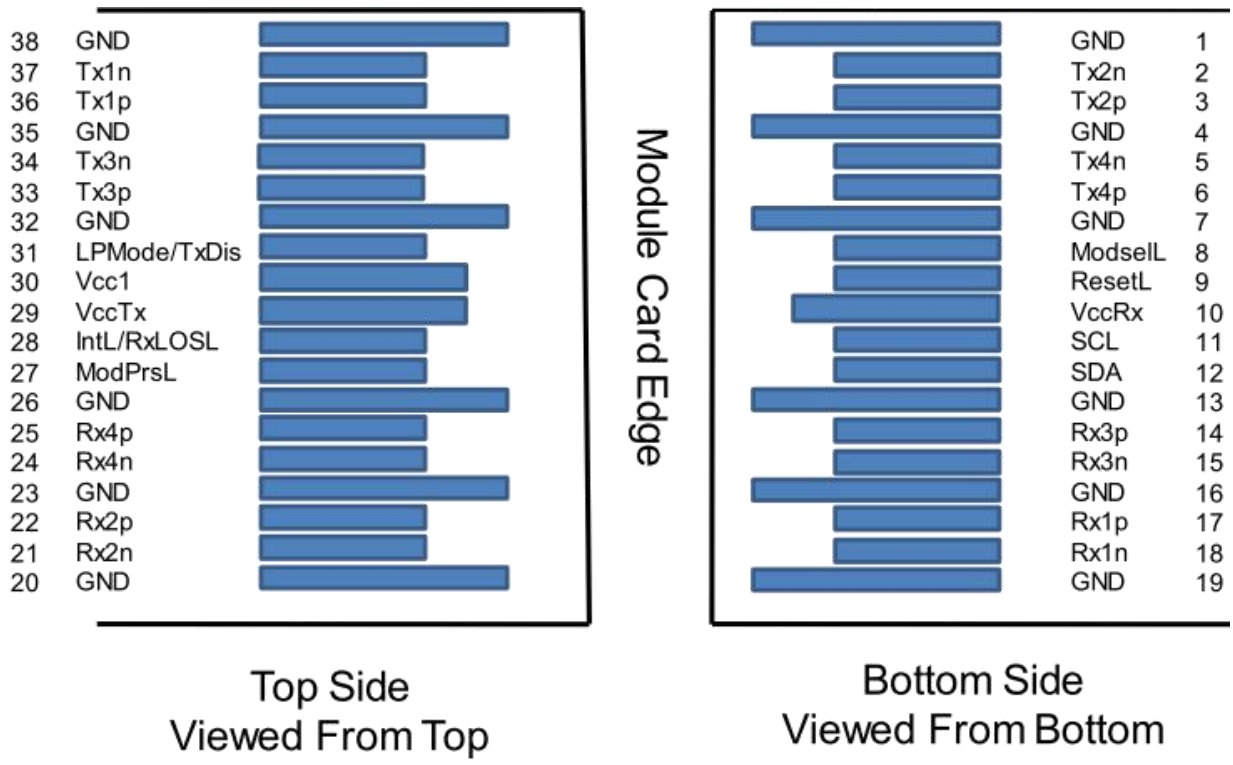
Optical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Center wavelength	L0	1272.55	1273.55	1274.54	nm	
	L1	1276.89	1277.89	1278.89	nm	
	L2	1281.25	1282.26	1283.27	nm	
	L3	1285.65	1286.66	1287.68	nm	
	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.09	nm	
Signaling rate, each lane			25.78125		Gb/s	
Side-mode suppression ratio	SMSR	30				
Total launch power	PT	8.0			dBm	
Average launch power, each lane	Pavg	2.0		6.0	dBm	
Extinction Ratio	ER	6.0			dB	
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			3.6	dB	

Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Transmitter reflectance	RT			-12	dB	
RIN20OMA	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Receiver						
Center wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.09	nm	
	L0	1272.55	1273.55	1274.54	nm	
	L1	1276.89	1277.89	1278.89	nm	
	L2	1281.25	1282.26	1283.27	nm	
	L3	1285.65	1286.66	1287.68	nm	
Signaling rate, each lane			25.78125		Gb/s	
Average Receive Power, each Lane		-30		-7	dBm	
Input Saturation Power (overload)，each Lane	Psat			-7	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity Average, each lane	SEN			-26	dBm	1
LOS Assert	LOSA	-40			dBm	
LOS Deassert	LOSD			-27	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:**Measured @25.78125Gbps, ER=8.2dB, BER=<5E-5, PRBS=2^{31}-1 NRZ**

Pin Diagram



Pin Descriptions

Pin	Symbol	Name/Description	Notes
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	

12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	

38	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1.GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2.VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2- wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met

ResetL:

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:

LPMode: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

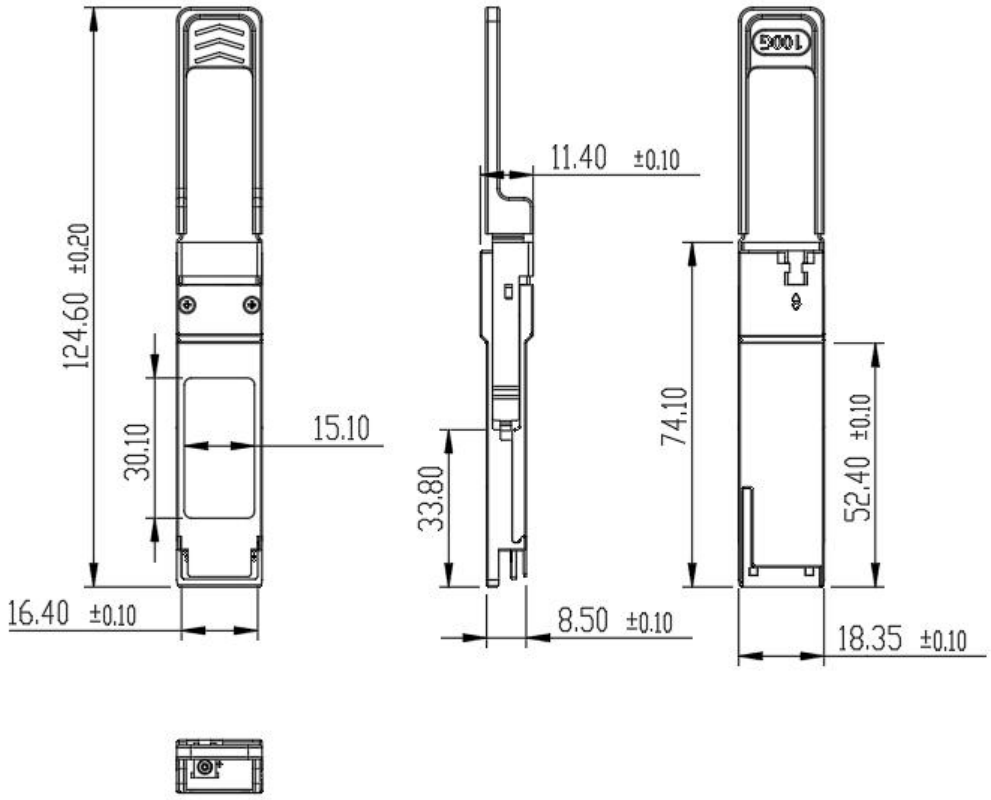
ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL:

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read .

Mechanical Specifications(Unit: mm)



Ordering information

Part Number	Product Description
QFP-BL23HG-80DC	100Gbps BIDI QSFP28 ZR4, LC, 80km, 0°C~+70°C, with DDM
QFP-BL32HG-80DC	100Gbps BIDI QSFP28 ZR4, LC, 80km, 0°C~+70°C, with DDM

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